METHOD AND CIRCUIT FOR OPTIMIZING POWER CONSUMPTION IN A FLIP-FLOP

Abstract of Disclosure

A flip-flop is disclosed. The flip-flop includes a first latch for receiving at least one bit and a second latch coupled to the first latch for storing the at least one bit from the first latch. The size of the second latch is minimized to reduce power consumption. The flip-flop also includes a multiplexor coupled to the first latch and to the second latch for outputting the at least one bit from the first latch, when a clock to the multiplexor is active and for outputting the at least one bit from the second latch when the clock is inactive. A system and method in accordance with the present invention optimize power consumption in a flip-flop through the use of a multiplexor for the output function. As a result, the size of the slave latch can be minimized, which reduces the overall power consumption of the device.